Final Report

December 31, 1994

Optoelectronic Technology Consortium
OETC

Sponsored by:

Defense Advanced Research Projects Agency
Microelectronics Technology Office

[PRE COMPETITIVE CONSORTIUM FOR OPTOELECTRONIC INTERCONNECT TECHNOLOGY]

DARPA Order No. 8371A

Issued by DARPA/CMO under Contract # MDA972-92-C-0072

Effective Contract Date: July 1, 1992

Contract Expiration Date: December 31, 1994

Lockheed Martin Electronics Laboratory
Syracuse, NY 13221

Issued: 31 May, 1996

OFFICE OF THE UNDER SECRETARY OF DEFENSE (ACQUISITION & TECHNOLOGY)
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1. Reference: DoD Directive 5230.24, Distribution Statements on Technical Documents, 18 Mar 87.

2. The Defense Technical Information Center received the enclosed report (referenced below) which is not marked in accordance with the above reference.

FINAL REPORT FOR OPTOELECTRONIC INTEGRATED TECHNOLOGY UNDER CONTRACT #MDA972-92-C-0072

3. We request the appropriate distribution statement be assigned and the report returned to DTIC within 5 working days.

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FOR THE ADMINISTRATOR:

Crystal Riley

1 Encl

CRYSTAL RILEY
Chief, Input Support Branch

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OTR (Reason)	DARPA/ETO (Controlling DoD Office Name)
DARPA/ETO (Assigning Office)	3701 N. Fairfax Dr Arlington VA 22203 (Controlling DoD Office Address (City/State/Zip)
Robert M. Glaze (Signature & Typed Name) Robert M. Glaze	24 Jun. 1996 (Date Statement Assigned)

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1. Summary

This is the final report prepared by Lockheed Martin Electronics Laboratory (LMEL) for ARPA in accordance with the provisions of Contract No. MDA972-92-C-0072, entitled "Optoelectronic Technology Consortium." The objective of this program was to develop, fabricate, integrate, and demonstrate the producibility of optoelectronic components for high-density/high-data-rate processors. This report details the progress on the LMEL tasks contributing to the development of the OETC 32-channel optoelectronic data link.

The OETC was an industry consortium of Lockheed Martin, AT&T, Honeywell, and IBM, supported by ARPA, to develop key optoelectronic components that advance interconnect technology beyond current cost, speed, and density barriers. OETC's structure included a Users Application Group and a Research Associates Group for continuous technology exchange and user feedback, combining both military and commercial perspectives, goals, and strategies.

The optoelectronic data bus was developed to meet the needs of future distributed workstation clusters and communication/memory intensive intelligence networks. By sharing the specialized talents and core technologies of the OETC member companies, this consortium advanced the technology, benefits, and use of optoelectronic links for connecting processors, clusters of processors, and I/O devices, over distances from a few to 100 meters. These links offer the advantage of combining low loss with high bandwidth for greater information capacity, small size with optical isolation to achieve higher spatial density, and parallel architecture to alleviate the bottleneck associated with existing metal interconnect technology.

Under OETC, twelve data busses were successfully demonstrated. Four were shipped to Lockheed Martin for insertion into a test bed, and eight were shipped by AT&T directly to IBM, Honeywell, and internal AT&T groups, for their own testing. In November 1994 at the final Users Group meeting, the OETC demonstrated a working 32-channel bus with data transmission rates of up to 622 Mbps per channel and bit error rates of better than $8x10^{-15}$. This data rate exceeds the program goal of 500 Mb/s and matches a key ATM/SONET data rate of importance in the data communications and telecommunications switching markets.

2. Task Objectives

The Lockheed Martin Corporation tasks were:

Task G.1 - Program Management
Provide a focal point for DARPA, the Steering Committee, and the User Applications Group; establish task descriptions and technical, cost, and schedule objectives for all consortium participants; organize program reviews for DARPA; and monitor technical progress and costs incurred for each major task and report to DARPA.

Task G.4 - Surface Emitting Laser Array Driver
Design, fabricate, and test parallel drivers for the SEL arrays developed by AT&T which includes a provision to automatically adjust the SEL drive current for variations caused by temperature changes and device aging.

Task G.5 - Waveguide Modulator Driver IC
Fabricate and test parallel drivers for the waveguide modulator arrays developed by Honeywell.

Task G.6 - Test-Bed Components Development
Specify , design, and develop or purchase all of the components for the OETC test-bed. Required components included a 32x4x4 crosspoint switch MCM, a MUX/DeMUX IC, Clock and Sync ICs, and processor/memory ICs.

Task G.7 - Test-Bed Integration
Design a 32-channel, 500 MHz data rate parallel optical data link using the optoelectronics components developed by the consortium. Fabricate and assemble the test-bed circuit boards, code and debug software for the model application, prepare a test plan, and evaluate the links and components developed by the consortium.

3. Technical Challenges

The major technical obstacles which had to be conquered for successful completion of the Lockheed Martin tasks were:

Task G.4 - Surface Emitting Laser Array Driver

A challenge to designing the laser driver was the lack of a good electrical model for the laser arrays. Since the laser driver IC was being designed at the same time as the first prototype lasers were being grown, a good electrical model for the laser was unavailable. The driver had to control the modulation currents between threshold and the desired upper level uniformly across the array. A controller had to be incorporated to adjust for variability caused by temperature fluctuations, aging, and differences in laser performances.

Task G.5 - Waveguide Modulator Driver IC

The challenge with the design of the driver IC was that the driver had to be designed simultaneously to Honeywell performing the waveguide modulator design. While there were no circuit models available to devind the capacitive load, the driver was required to operate at high speed with a good extinction ratio (turn on/turn off). The unknown capacitive load created a challenge for designing the driver to meet the speed objective.

Task G.6 - Test-Bed Components Development

Individual components each represented their own unique challenges for development.

The first component to be developed was a 32x4x4 cross point switch. The requirement was to get the broadest signal distribution possible using available TriQuint chips. The challenge was to achieve the interconnectivity desired without causing a delay in signal transmission. Due to the quantity of power dissipate by the cross point chips, the MCM had to be designed (laid out) on a high thermal conductivity substrate material (Lanxide) without the benefit of extensive design experience. The solution was to engage the GE Corporate Research & Development center as a consulting resource for the design activity.

The next component was the MUX/DEMUX IC. The challenge here was to develop a way to take a low speed CMOS signal, replicate it in an uncorrelated manner, and create a differential ECL signal on each of 32 lines at 500 Mbps (16 Gbps aggregate), for transmission. At the output of the receiver, the differential ECL output was demultiplexed and converted to a single ended CMOS for storage in memory. The incoming signal format was derived from a microprocessor. Data was generated at a lower rate and then replicated with 10 cycles of this lower data rate to meet the final specified data volume requirement. A significant challenge was synchronizing the related data to meet the format requirements.

The next component was the clock/synchronizer IC's. The challenge here was designing a phase lock loop to achieve the speed and formatting needed for the data stream described above.

Finally, the last component development was for the processor/memory IC's. The challenge was to be able to handle the large volume of data storage needed to do a FIFO (First In First Out) comparison of the data stream - (input matched against output). In order to meet the data volume and speed requirements, the power consumption and system board size in this section of the Test Bed became a significant demand.

Task G.7 - Test-Bed Integration

The challenge here was simply to integrate the unique components from four major technical entities - AT&T, IBM, Honeywell and LMEL (formerly GE Electronics Laboratory) into a single test bed. The best bed was to demonstrate that optical systems could overcome the electrical/electronic bottlenecks for linkage between distributed work stations.

4. General Methodology

The optical link design was specified based on the power budget calculations (Figure 1), the laser operating specifications (Figure 2 and Table 1), transmission experiments accomplished by AT&T and IBM, and conferences with the component suppliers. The link specification , Table 2, was circulated among OETC members and agreed upon in April 1993

4.1. Surface Emitting Laser Array Driver

This circuit as designed has the capacity to set the laser threshold from 1 to 6 mA and the upper modulation limit from 7 to 10 mA. It provides modulation currents between 1 and 9 mA at a data bandwidth of 1 Gbps (Manchester encoded). The design consisted of modulation and threshold FETs, a differential input, and a differential to single output conversion stage that directly drives the laser. Analog bias control circuits establish the threshold current (low level output) and the modulation current (high level output).

These laser drivers were fabricated in July of 1993, delivered in October of 1993. There were 60 candidate circuits that passed all DC test requirements. Of these, 40 were delivered to AT&T for assembly. AT&T packaged their lasers with the drivers and returned the assembled units to LMEL (then GE Electronics Lab) for testing in January 1994. (The drivers could not be fully tested without final assembly with the lasers.) The transmitters worked when tested at LMEL, but there was a problem with the feedback system. Oscillation due to feedback capacitance was discovered in the drivers control current (<lmA). In all, 16 transmitter modules were built, and 12 operated from that build.

4.2. Waveguide Modulator Data Interface.

Due to the unproven performance of the vertical cavity surface emitting lasers at the project inception, an alternative design for the transmitter module was incorporated. The waveguide modulator developed by Honeywell was driven by a driver circuit designed using LMEL IR&D funds. The contract statement of work calls for testing the Honeywell modulators using standard lab equipment. The layout and design of the Mach-Zehnder modulator driver was completed and sent to TriQuint Semiconductor for reticle assembly and fabrication on 7/1/93. The design was a push-pull, dual complementary driver with each output having equal maximum voltage swings. The complementary outputs were capacitively coupled and separately biased. HSpice simulations confirmed that the driver would be functional with modulators based on Honeywell's latest electrical specification. The assumed waveguide modulator array required a modulation voltage between 3 and 4 volts for operation. Circuit modifications to the modulator driver were made to include separate adjustable supplies on the output buffers to achieve the desired modulation voltage across all elements of the modulator array. Final simulations using Quicksim and HSpice verified the Manchester encoder circuitry and the ability to modulate at 1 Gbps data rate with a voltage swing between 3 and 4 volts. The modulator driver configuration and simulated output are illustrated in Figure 4 and 5.

4.3 Test-Bed Components Development

The Modulator drivers were fabricated, tested and delivered to Honeywell for integration with their modulators.

4.3.1. Crosspoint Switch.

A single integral module design approach was chosen. Using the General Electric Corporate Research and Development (GE-CR&D) high density interconnect (HDI) process, a special integral substrate material, Lanxide, was chosen. Lanxide was selected to be able to deliver the thermal conductivity required by the high speed crosspoint switch assembly. The design also allowed the OETC transmitter and receiver module to be surface mounted o the periphery of the substrate. Thermal analysis was carried out after power figures, footprints, and preliminary floor plans were defined and provided to GE-CR&D.

At month 22 of the 30 month program, module testing costs were higher than had been planned. The ARPA customer agreed with this decision primarily because none of the users were asking for the switch. Since the funds were depleted, this switch work was not completed. Work was stopped at the customer's direction.

A layout for the HDI module was completed and analyzed. This effort was also suspended at the customer's direction due to higher than expected module testing costs.

4.3.2 MUX/DEMUX IC.

The multiplexer (MUX) and the demultiplexer (DEMUX) circuit design, simulation, and I/O placement were completed. Block diagrams of the MUX and DEMUX are displayed in Figures 6 and 7, respectively. The MUX takes data from a 64-bit wide, single-ended, 25 MHz, CMOS compatible bus and converts it to a 32-bit wide fully differential, 500 Mbps NRZ, ECL compatible data bus. The DEMUX takes in a 500 Mbps, 32-bit wide fully differential, ECL compatible, NRZ data stream, along with a 500 MHz timing reference, and converts them to a 64-bit wide, single-ended, 25 MHz, CMOS compatible data bus along with a timing reference. A design review was held at TriQuint on June 7-8, 1993 to resolve computer interface and control issues. Logic simulation of the MUX/DEMUX confirmed the design functionality, and the MUX/DEMUX designs were released for fabrication on 7/1/93. Fabrication was completed. The multiplexer was tested to specification, it missed specified performance because of an on-chip clock's internal phased lock loop problem. The problem was corrected, redesigned and another lot fabricated at TriQuint (they provided support for this since the clock's problem was theirs. This refabrication started in March of 1994 and the circuits were tested in July of 1994). From this second fabrication 16 chips passed DC probe specs. These 16 circuits were available to populate the test bed, but the test bed work was suspended. No further effort was applied.

4.4. Test-Bed Integration.

The test bed design was completed. All of the required parts were ordered. It was determined while awaiting parts delivery that all of the funds were depleted. At customer direction, the Test Bed Integration task was terminated and the parts on order were canceled.

5. Technical Results

The Tx module connects to the Rx module using a 32-fiber multimode ribbon cable. The Tx module contains a 32-element VCSEL array, at 850 nm, optically coupled to the fibers through a fiber-array block. The Tx module also includes drive electronics to convert the incoming digital electrical signals into appropriate modulated currents for the individual laser diodes. The Rx module couples optical signals onto an array of 32 GaAs MSM detectors on a single chip, 32-channel, optoelectronic integrated circuit (OEIC) receiver array. The Tx module accepts and the Rx module outputs standard emitter coupled logic (ECL) levels.

Data at 500 and 622 Mbps were transmitted over optical fiber ribbon cables of lengths up to 100 meters. The bit error rate (BER) was less than 8×10^{-15}. Channel-to-channel uniformity of the transmitter optical output was better than ± 152 mW. The Tx dissipated an average of 7.6W, and the receiver dissipated an average of 2.5W. The bus latency was less than 2.5 ns excluding time of flight, and the output skew was less than ± 250 ps. The data bus has operated over a temperature range of 0° - 70°C.

OETC. We submitted a request to ARPA for a revised Statement of Work where we would substitute the extensive, unanticipated module level testing we had done, for the originally intended testbed demonstration. The COTR indicated that no additional funds were available so we had to complete what we could within the available funding.

6. Important Findings and Conclusions

The demonstration identified the following:

- Up to 622 M bits see could be transmitted over 32 channels.
- Transmission distances of 100 meters with 300 meters possible.
- Laser stability indicated that feedback in the driver circuits would not be required.
- Lower power and smaller size with accompanying reduced cost was available by eliminating the feedback.
- Ultimately a smaller transmitter package could be created achieving lower cost for the transmitter.

FIGURE 1

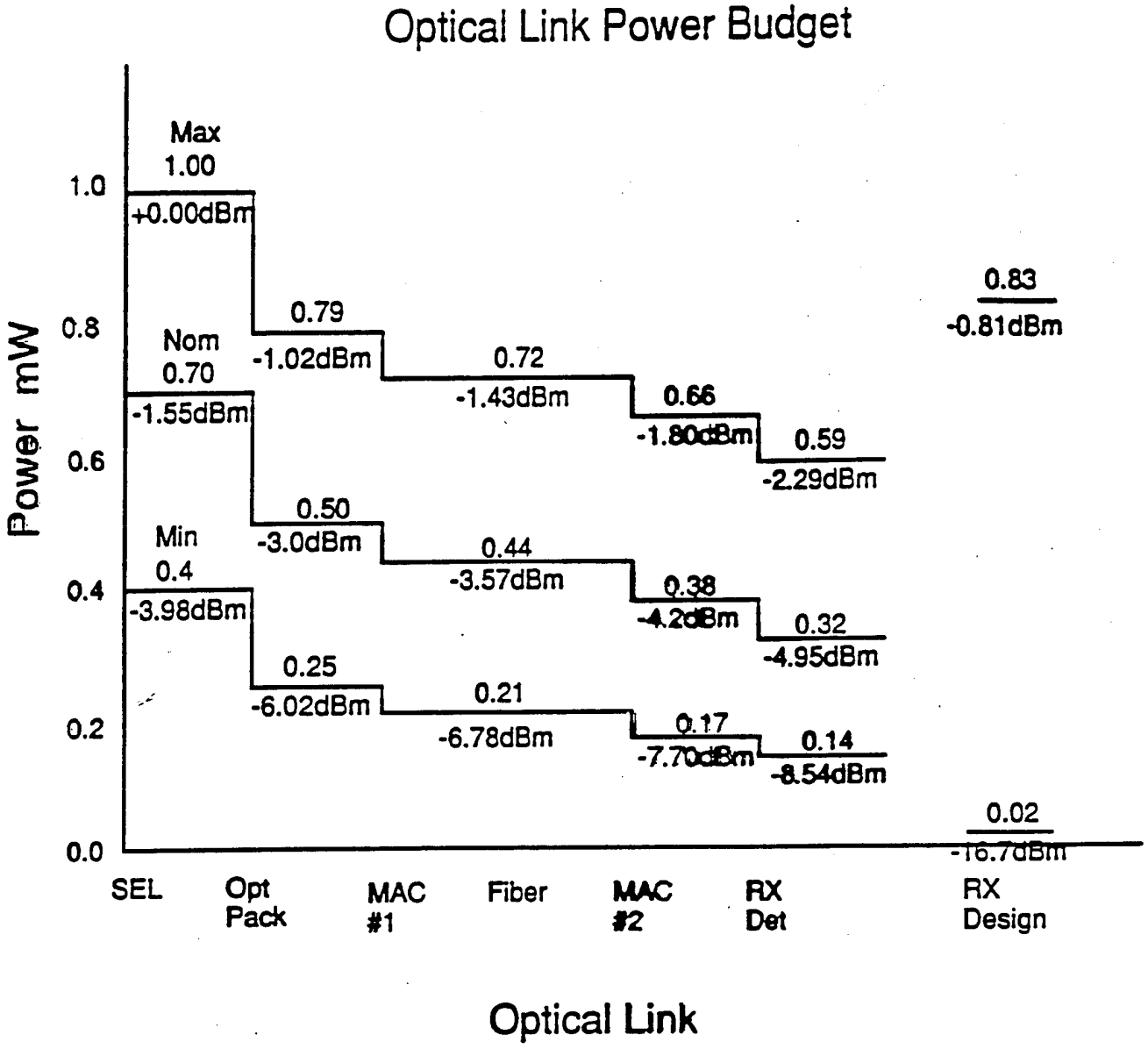

Optical Link Power Budget
Power mW
1.0
0.8
0.6
0.4
0.2
0.0
Max
1.00
+0.00dBm
Nom
0.70
-1.55dBm
Min
0.4
-3.98dBm
0.79
-1.02dBm
0.72
-1.43dBm
0.66
-1.80dBm
0.59
-2.29dBm
0.50
-3.0dBm
0.44
-3.57dBm
0.38
-4.2dBm
0.32
-4.95dBm
0.25
-6.02dBm
0.21
-6.78dBm
0.17
-7.70dBm
0.14
-8.54dBm
0.83
-0.81dBm
0.02
-16.7dBm
SEL
Opt Pack
MAC #1
Fiber
MAC #2
RX Det
RX Design
Optical Link

FIGURE 2

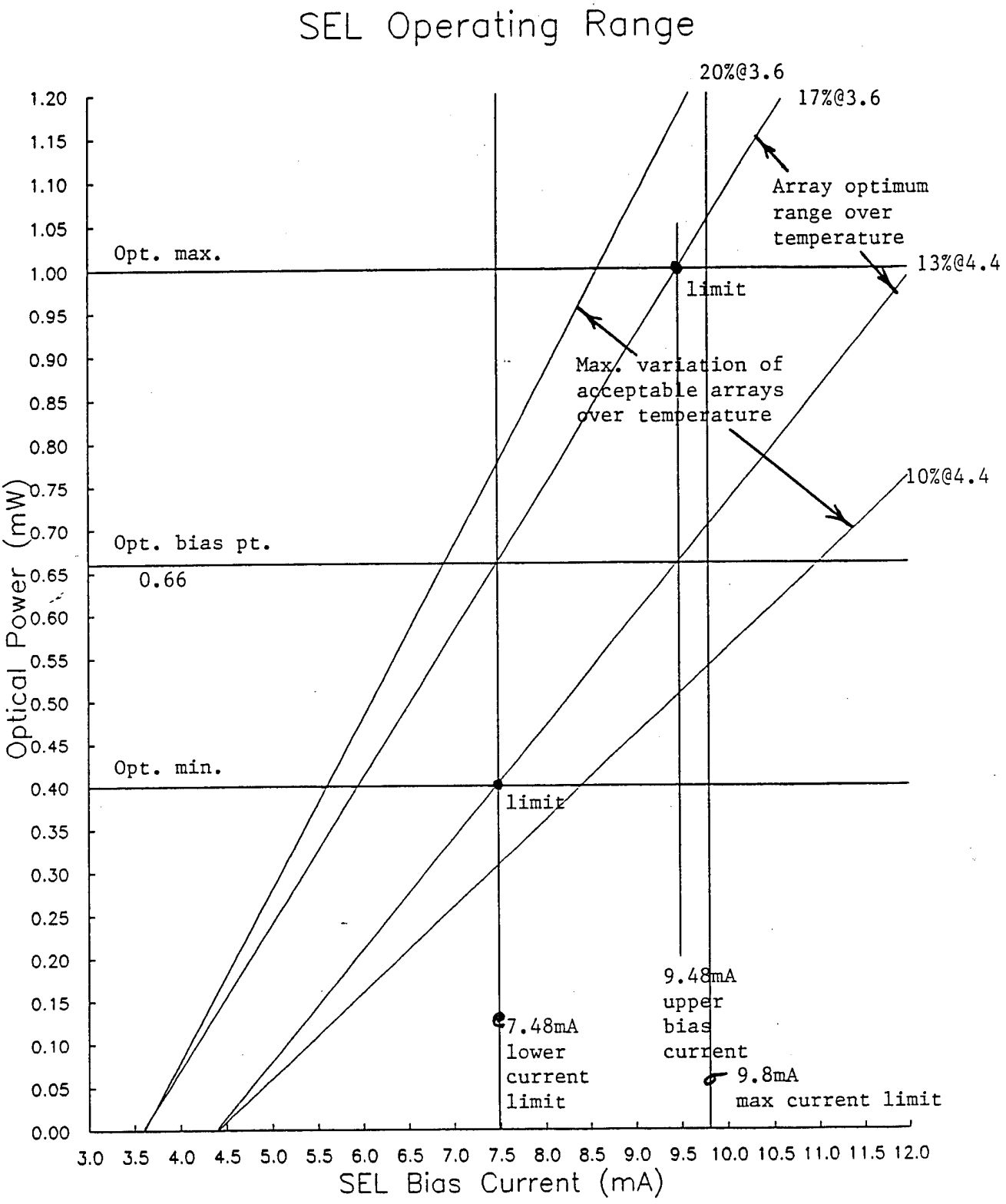

SEL Operating Range
20%@3.6
17%@3.6
Array optimum range over temperature
13%@4.4
Opt. max.
limit
Max. variation of acceptable arrays over temperature
10%@4.4
Opt. bias pt.
0.66
Opt. min.
limit
9.48mA upper bias current
7.48mA lower current limit
9.8mA max current limit
Optical Power (mW)
SEL Bias Current (mA)
1.20
1.15
1.10
1.05
1.00
0.95
0.90
0.85
0.80
0.75
0.70
0.65
0.60
0.55
0.50
0.45
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.00
3.0 3.5 4.0 4.5 5.0 5.5 6.0 6.5 7.0 7.5 8.0 8.5 9.0 9.5 10.0 10.5 11.0 11.5 12.0

TABLE 1

Laser Operating Specifications

SEL	MIN	NOM	MAX		
Threshold Current ±10%	3.6mA	4.0mA	4.4mA		
Bias Current	3.0mA	3.3mA	3.6mA		
Modulation Current "1"	7.6mA	8.7mA	9.8mA		
SEL Optical Power "O" (-10dBm)	<100µW	<100µW	<100µW		
SEL Optical Power "1"	0.4mW	0.7mW	1.0mW		
Coupling Loss (SEL to fiber) [-1.5±0.5dB]	-2.0dB	-1.5dB	-1.0dB		
Optical Power Before Conn "0"	<63µW	<71µW	<79µW		
Optical Power Before Conn "1"	252µW	499µW	794µW		
Conn Loss [-0.6±0.2dB]	-0.8dB	-0.6dB	-0.4dB		
Optical Power After Conn "0"	<52µW	<62µW	<72µW		
Optical Power After Conn "1"	210µW	435µW	724µW		
Fiber Loss Negligible					
Conn Loss [-0.6±0.2dB]	-0.8dB	-0.6dB	-0.4dB		
Optical Power After Conn "0"	<44µW	<54µW	<66µW		
Optical Power After Conn "1"	174µW	379µW	660µW		
RX Reflection Loss [-0.75dB±0.25dB]	-1.0dB	-0.75dB	-0.5dB		
Optical Power @ RX "0"	<35µW	<45µW	<59µW		
Optical Power @ RX "1"	139µW	318µW	588µW		
RX Loss [-5.75±3.25dB]	-9.0db	-5.75dB	-2.5dB		
RX Sensitivity BER=10-9	-21dBm	-22dBm	-23dBm		
Net RX Sensitivity	-12dBm	-16.25dBm	-20.5dBm		
Optical Power Margin	+3.4dB	+11.2dB	+18.2dB		
GE Version #3 2/4/93					

Table 2. Optical Link Design Specifications:

AT&T Surface Emitting Lasers

Transmitter: Singlemode VCSEL		**Min**	**Nom**	**Max**
Data Rate, MBaud		950	1000	1050
Wavelength, nm		830	840	850
Spectral Width, nm			1.0	
Optical Power, mW peak				
1		0.4	0.7	1.0
0		0.0	0.05	0.1
Rise/Fall Time (10-90%), ns			0.250	0.400
Threshold Current, mA		3.6	4.0	4.4
Bias Current, mA			4.0	
Drive Current above I_{th} to reach rated output power, mA		4.0		
Forward Voltage, V			3.5	4.5
Extinction Ratio, dB		6	10	
Quantum Efficiency, mW/mA		0.1	0.15	0.2
Relative Intensity Noise, dB/Hz		-115	-125	
Optical Crosstalk, dB	<-30			
Input Signal Interface		ECL		
Operating Temp. Range,_C		0		70
Power Dissipation, Watts [1]			6.0	
Data Skew, ps [1]			100	
Data Jitter, ps [1]			40	

[1] Values include power dissipation, skew, and jitter for laser driver

Honeywell Modulator

Transmitter: External Modulator	**Min**	**Nom**	**Max**
Data Rate, MBaud	950	1000	1050
Wavelength, nm	830	840	850
Spectral Width, nm		1.0	
Optical Power, mW			
peak @ laser		150	
peak @ link			
1	0.4	0.4	1.5
0		0.03	
Rise/Fall Time (10-90%), ns		0.400	0.400
Modulation Voltage, V		4.0	5.0
Bias Voltage, V	2.0		8.0
Extinction Ratio, dB	6	10	
Relative Intensity Noise @link, dB/Hz	-115	-125	
Optical Crosstalk, dB <-30			
Operating Temp. Range, _C	0		70
Data Skew, ps		100	
Data Jitter, ps		40	

Table 2. Optical Link Design Specifications (con't)

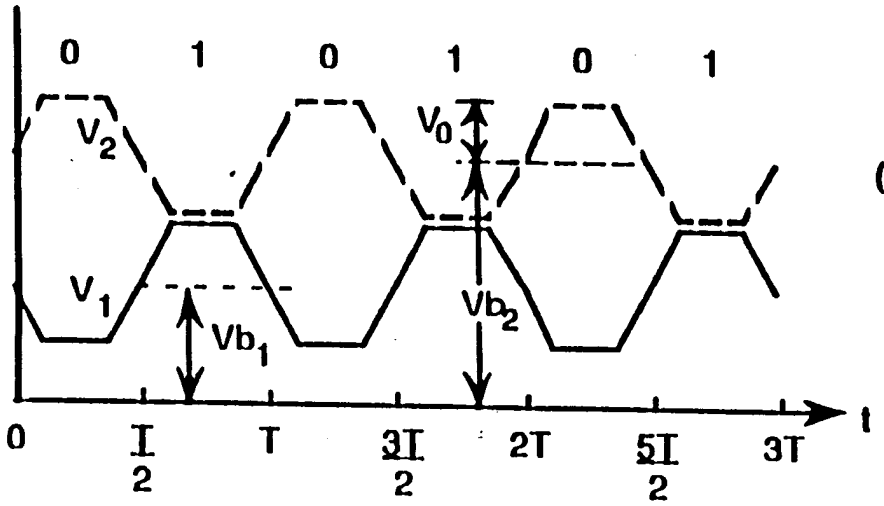
Waveguide: GI Multimode Fiber	**Min**	**Nom**	**Max**
Core Diameter, mm	59.5	62.5	65.5
Cladding Diameter, mm	123	125	127
Coating Diameter, mm		130	140
Operating Wavelength, nm		850	
Bandwidth, MHz-km	160		400
Attenuation, dB/km	2.7		3.2
Numerical Aperture	0.260	0.275	0.290
Zero Dispersion Wavelength, nm	1320		1365
Zero Dispersion Slope, ps/km-nm^2			0.097
Group Refractive Index		1.496	
Coupling Efficiency, %	83	87	93
Length, m	0.1	10	100
Data Skew, ps		15	

IBM MSM-PD/MESFET Receiver

Receiver: Transimpedance Amp RX		**Min**		**Nom**	**Max**
Detector Responsivity, mA/mW				0.35	
Detector dark current, nA				5.0	
Detector Capacitance, pF				0.15	
Active Area, mm			80 mm x 120 mm rectangle		
FET gate-drain capacitance, pF				0.02	
FET gate-source capacitance, pF				0.16	
FET transconductance, mS				3.5	
FET gate leakage current, nA			2.0		
FET channel noise factor				1.76	
1/f noise frequency, MHz				100	
Maximum Optical Input, mW pk-pk		16[2]			625
Optical Crosstalk, dB	<-30				
Optical Dynamic Range, dBm				16	
Low Frequency (-3 dB), MHz				1.0	
Bandwidth, MHz		670		900	1120
Input Setup & Hold Time, ps	450				
Output Delay, ps				1000	1500
Clock to Data Delay, ps				1000	
Input Rise/Fall Time, ps				300	400
Clock Period, ps		1900		2000	2100
Clock Pulse Width, ps		900		1000	1100
Data Skew, ps				50	
Data Jitter, ps				50	
Voltage Output - High, V		-1.0		-0.75	
Voltage Output - Low, V				-1.9	-1.6
Power Dissipation, Watts				2.5	
Operating Temp. Range, _C		0			70
Bit Error Rate	10^{-9}		10^{-15}		

[2] For minimum bit error rate, 10^{-9}

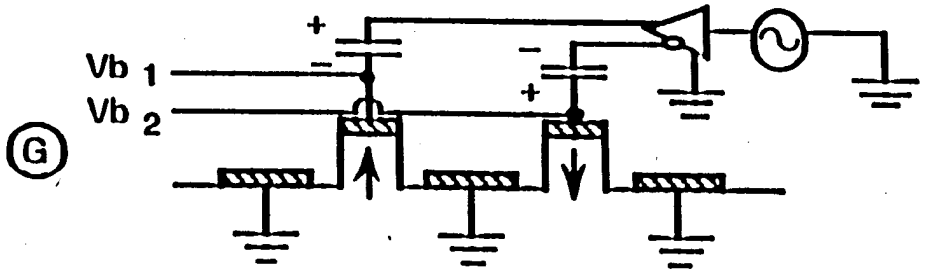
FIGURE 4

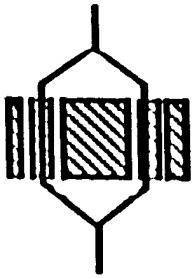


(vi) Push-Pull, dual (complementary) driver with equal maximum voltage swings with unequal biases. (Case G).

B910196-13

FIGURE 5





Push-Pull, dual driver, capacitively coupled, separately biased configuration

B910196-12